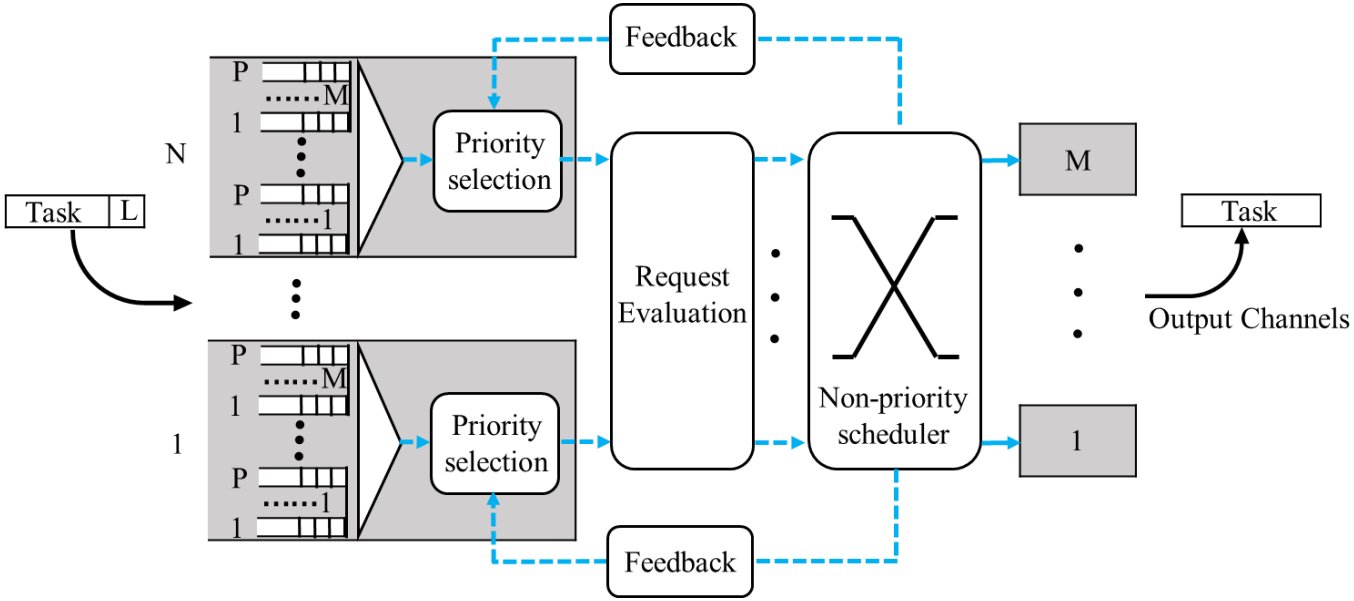

Work-in-Progress: A Flattened Priority Framework for Mixed-Criticality Real-time Systems

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Motivation

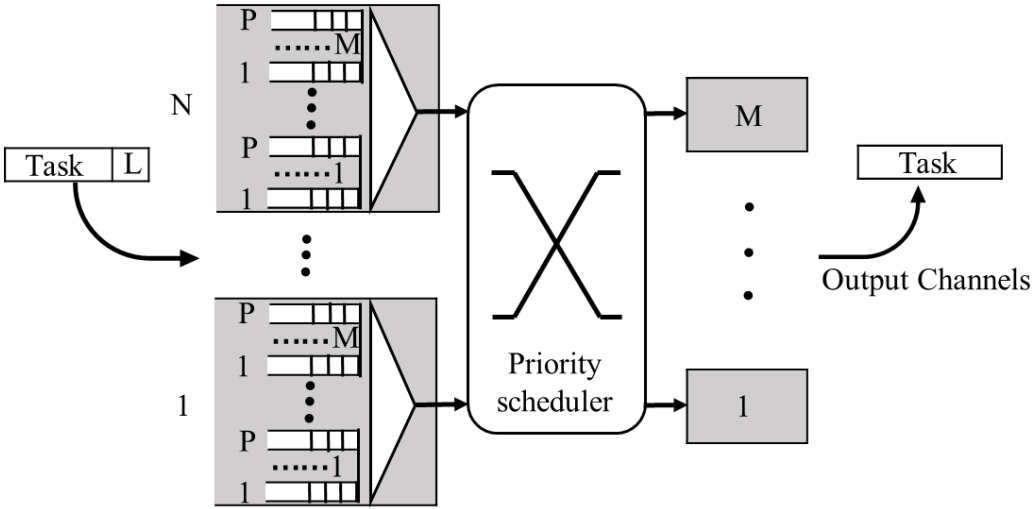
Mixed Criticality Systems

- Ever-increasing integrated services
  - Diverse performance objectives and multiple traffic characteristics
    - E.g. Industrial Ethernet (802.3 Ethernet, time-critical services)
- Fast-growing deployment on smart devices
  - Limited Resource
    - E.g. Virtex-7 XC7VX485T FPGA (o
- Central component: priority schedulers
  - General NP-complete
    - E.g. Scheduling problem of deadline guaranteed packets[1]

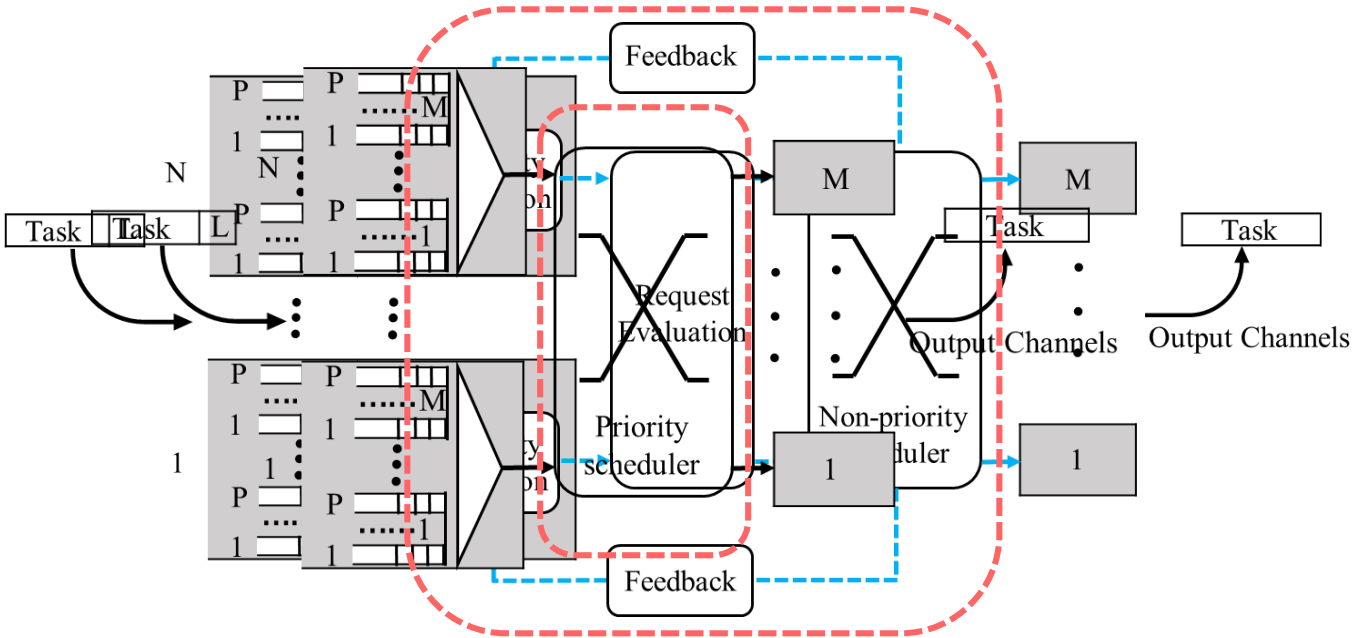
[1] B. Zhang, X. Wan, J. Luo, and X. Shen, "A nearly optimal packet scheduling algorithm for input queued switches with deadline guarantees," IEEE Transactions on Computers, vol. 64, no. 6, pp. 1548–1563, 2015

A general priority scheduling framework

- P priorities such as criticality levels, deadlines, QoS
- N input channels: load tasks with multiple priorities
- M output channels: processors, memory, I/O
- L occupying time



Our flattened priority framework



A priority scheduler is simplified into a nonpriority one!

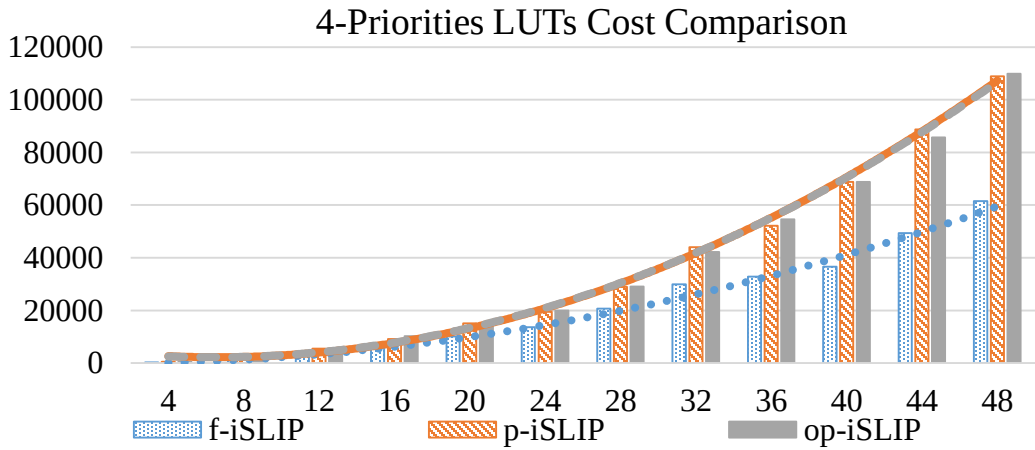
Case study on Industrial Ethernet switches

Industrial Ethernet Switches

- A nonpriority scheduler, well-known as iSLIP[2]
- Two modified versions of iSLIP for priority schedulers
  - one denoted by p-iSLIP[2]
  - one denoted by op-iSLIP[3]

Our priority scheduler, f-iSLIP :
Flattened priority framework + iSLIP

LUTs cost: 30%~50% reduction!



[2] N. McKeown, "The islip scheduling algorithm for input-queued switches," IEEE/ACM transactions on networking, vol. 7, no. 2, pp. 188–201, 1999
[3] A. R. Minagar and S. M. Safavi, "The optimized prioritized islip scheduling algorithm for input-queued switches with ability to support multiple priority levels," in *Telecommunications, 2003. ICT 2003. 10th International Conference on*, vol. 2. IEEE, 2003, pp. 1680–1685.

Conclusion & Future works

Summary

- A general framework to transform a non-priority scheduler into a priority one
- A case study on Industrial Ethernet switches to illustrate its potentialities for resource-efficient schedulers

Next ?

- Formal analysis on iterative convergence for maximal matches
- More case studies on the tradeoff for performance and resource efficiency

Thank you !

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